BK3431S Datasheet

Single Mode Bluetooth Low Energy SoC

Preliminary Specification

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Table of Contents

1 General Description

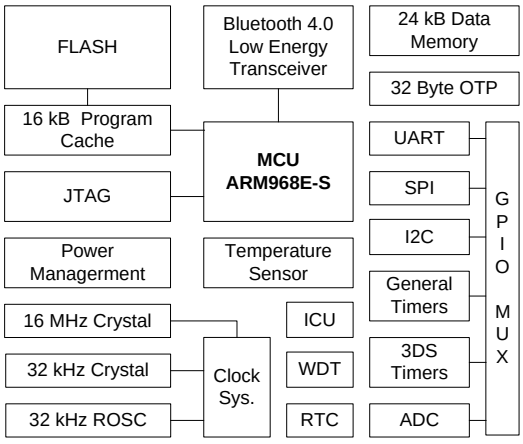
1.1 Overview

The BK3431S chip is a highly integrated SoC with Bluetooth 4.0 low energy single mode transceiver. It integrates a high-performance 2.4GHz RF transceiver, rich features baseband, ARM968E-S MCU and various peripheral IOs. It has embeddd FLASH and 24 kByte RAM to enable programmable protocol and profile to support customized applications.

The BK3431S has 32 Byte OTP and internal encryption logic for user program security.

The BK3431S has dedicated 4 channel PWM timers for 3D glasses application, where all 4 timers are synchronized in both phase and frequency.

1.2 Block Diagram



1.3 Application

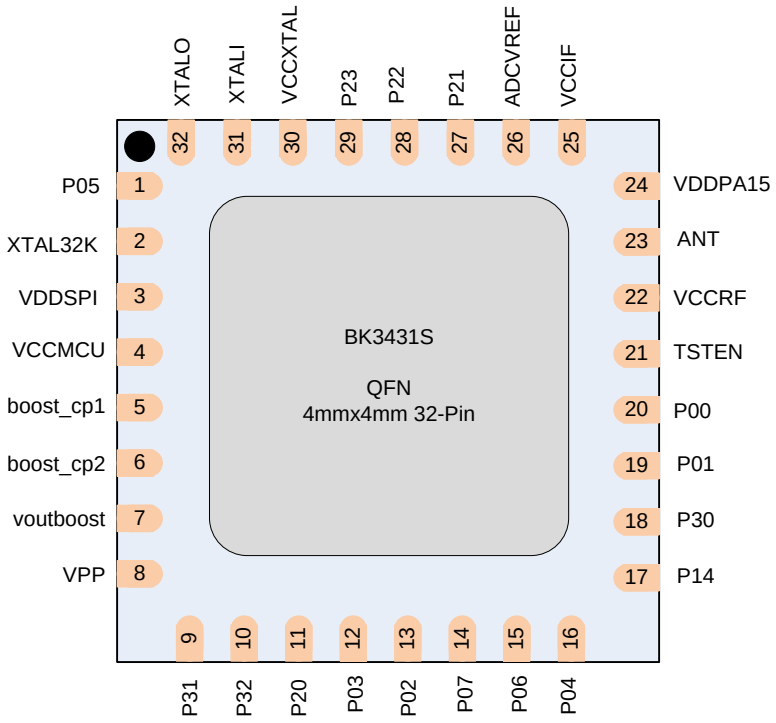
- HID Application
- Lighting Control
- Wireless Sensor Networks
- 3D Glassed
- Proximity and Find Me

1.4 Features

- Bluetooth 4.0 Low Energy
- Operation voltage 1.9 V to 3.6 V
- Integrated 32 Byte OTP
- -89 dBm Sensitivity
- Maximum 4 dBm output power
- ARM968E-S MCU Integrated
- 24 kByte data RAM
- I2Cs, SPI and UART Interface
- Six PWM Timer
- Temperature Sensor
- 8-channel 8-bit General ADC
- 4-channel 3DS PWM Timer
- Low Power Real Time Counter
- 3 uA in Deep-sleep Mode
- 9 uA in All Retention Mode
- 13 mA Transceiver RX Active
- 13 mA Transceiver TX Active
- 8 mA for MCU at 16 MHz
- QFN 4x4 32-pin

2 Pin Information

The pin assignment for QFN32 package is shown in picture below. The BK3431SQN32D has 8 Mbit FLASH inside.



NO	Name	Description
1	P05	General I/O, or MOSI for SPI, SO_FLA
2	XTAL32K	The input of 32K crystal oscillator
3	VDDSPI	The output of digital LDO
4	VCCMCU	3V power supply
5	boost_cp1	Boost function PIN. Add 100nF cap between boost_cp1 and boost_cp2
6	boost_cp2	Boost function PIN. Add 100nF cap between boost_cp1 and boost_cp2
7	voutboost	The output of boost
8	VPP	The 6V power supply of OTP,it can be used when download
9	P31	General I/O, or input of ADC1
10	P32	General I/O, or input of ADC2
11	P20	General I/O, or UART TX

12	P03	General I/O, or 3DS_PWM[3], I2C1.SDA, WP_FLA
13	P02	General I/O, or 3DS_PWM[2], I2C1.SCL, HOLD_FLA
14	P07	General I/O, or SPI_NSS, CSN_FLA
15	P06	General I/O, or MISO for SPI, SCK_FLA
16	P04	General I/O, or SPI_SCK, SI_FLA
17	P14	General I/O, or enable for PWM4
18	P30	General I/O, or input of ADC0
19	P01	General I/O, or 3DS_PWM[1]
20	P00	General I/O, or 3DS_PWM[0]
21	TSTEN	Enable the testting function of memory
22	VCCRF	3V power supply
23	ANT	The input of RF
24	VDDPA15	The output of PA ldo
25	VCCIF	3V power supply
26	ADCVREF	The output of reference voltage of ADC. It can be connected to a cap on the board
27	P21	General I/O, or UART RX
28	P22	General I/O, or clock for I2C0
29	P23	General I/O, or data I/O for I2C0
30	VCCXTAL	3V power supply
31	XTALI	The input of 16M crystal oscillator
32	XTALO	The input of 16M crystal oscillator

3 Function Description

3.1 Memory Address Mapping

	Start Address	End Address	Total (Bytes)
Program Memory			
Flash space	0x00000000	0x0003FFFF	4M maximum
Data Memory			
SRAM	0x00400000	0x00405FFF	24K
AHB Peripheral			
ICU	0x00800000	0x0080FFFF	64K
FLASH CONTROL	0x00820000	0x0082FFFF	64K
AHB2APB	0x00F00000	0x00FFFFFF	1M
APB Peripheral			
WDT	0x00F00000	0x00F000FF	256B
PWM	0x00F00100	0x00F001FF	256B
SPI	0x00F00200	0x00F002FF	256B
UART	0x00F00300	0x00F003FF	256B
I2C0	0x00F00400	0x00F004FF	256B
GPIO	0x00F00500	0x00F005FF	256B

RTC	0x00F00600	0x00F006FF	256B
ADC	0x00F00700	0x00F007FF	256B
BT 3DS	0x00F00800	0x00F008FF	256B
I2C1	0x00F00900	0x00F009FF	256B
Timer	0x00F00A00	0x00F00AFF	256B
XVR	0x00F10000	0x00F1FFFF	64K
CEVA BT IP	0x00F20000	0x00F2FFFF	64K

3.2 Interrupt and Clock Unit

The MCU core clock can be selected from three clock sources: 32 kHz clock, 16 MHz clock and maximum 96 MHz clock from DPLL.

The ARM968E-S supports two interrupt level. The FIRQ has higher priority than nIRQ. In the BK3431S, all peripheral interrupts are nIRQ except the Bluetooth transceiver. All interrupt can be enabled, disabled, and cleared. There are two low power modes: MCU stop and deep sleep, and any interrupt can be configured to be a wake up source to let MCU exit low power mode.

3.3 GPIO

All the GPIO ports can be used for general I/O with selectable direction for each bit, or these lines can be used for specialized functions.

3.4 ADC

An 8-bits SAR-ADC is integrated in the BK3431S. Total 8 channels can be selected used for ADC transfer. The ADC supports continue mode and single transfer mode, and the sample rate can be 1 kHz to 32 kHz. In single transfer mode, it will generate interrupt every time after transform.

The ADC has four work modes they are sleep mode, single mode, and software mode and continue mode.

In single mode, the ADC will enter idle mode when transfer is done and waiting MCU to read the result. You should write mode=1 again for another transfer.

In software mode, the interrupt will be triggered after transfer is finished. The interrupt will be cleared after MCU read, and then the transfer will start again.

In continue mode, the ADC will work at the sample rate set by register. The sample rate can be calculated by the next formula:

F_sample = input ADC clock/(2^(ADC_CLK_RATE+2) / 36(or 18))

The highest sample rate is 32 kHz。

The local interrupt flag of ADC need not be cleared by software; it will be set after transform and be cleared after the result has been read out. But the ADC INT stored in ICU should be cleared after the ADC INT service finished.

The range of input voltage is from 0v to 1.5V. If the input voltage more than 1.5V, a resistor can be added to decrease the input voltage like the next diagram.

There are eight GPIO can be ADC input, whose voltage is equal the ADC read out divided with 448 and the saturate voltage is 1.5 volt.

3.5 UART

The UART interface has 128 bytes FIFO for both TX and RX. It will generate interrupt request when there is risk or event of FIFO underflow or overflow. For the RX, it will generate interrupt if found parity bit check error or stop bit check error.

When the UART RX line goes from idle state (‘HIGH’) to active state (‘LOW’) for a set UART clock cycle, it will generate wake up interrupt to activate MCU clock.

3.6 I2C-SMBus

The I2C I/O interface is a two-wire, bi-directional serial bus. The I2C is compliant with the System Management Bus Specification, version 1.1, and compatible with the I C serial bus. Reads and writes to the interface by the system controller are byte oriented with the I2C interface autonomously controlling the serial transfer of the data.

Data can be transferred at up to 1/10th of the system clock as a master or slave (this can be faster than allowed by the I2C specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation.

The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free.

3.7 SPI

The Enhanced Serial Peripheral Interface (SPI) provides access to a flexible, full-duplex synchronous serial bus. SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slaves.

There are four pins for SPI interface. The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI is operating as a master and an input when SPI is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI is operating as a master and an output when SPI is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

In slave mode, the data on MOSI are sampled at the middle of period of every bit. In master mode, the data on MISO are sampled at the last clock period to acquire the maximal setup time.

3.8 General PWM Timer

There are six timers, all of which can works as PWM waveform generator. These timers can work with either low speed 32 kHz clock or high speed 16 MHz clock. The PWM waveform can be output to GPIO to drive external device such as LED.

3.9 3D Glass PWM Timer

It has four synchronized timer in both phase and frequency, to control the left and right shutter with differential PWM waveform. The timer has 1/16 us phase accuracy and maximum 262 ms period.

3.10 Watch dog

The watch dog is used to reset the whole chip when the firmware runs out of order.

4 Electrical Specifications

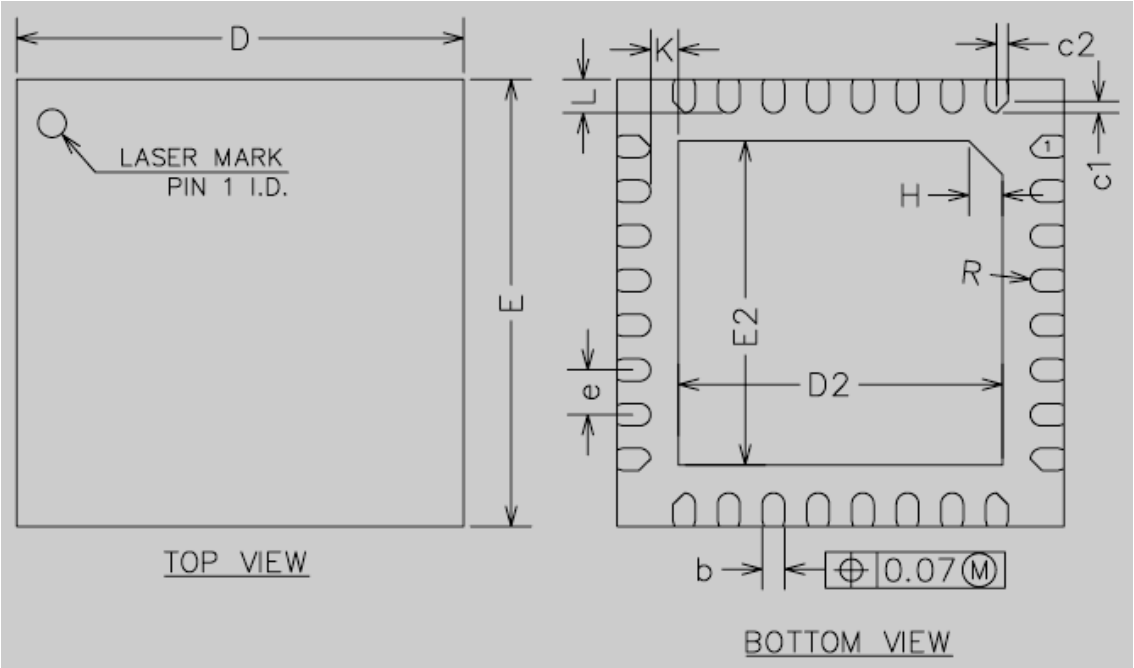
4.1 DC Performance

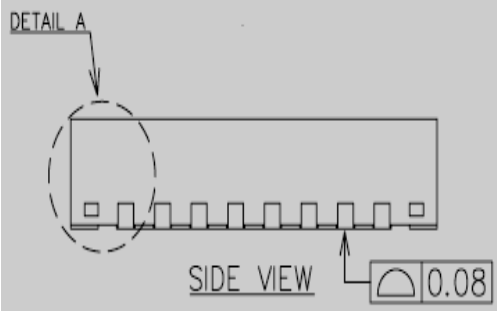
Name	Parameter (Condition)	Min	Typical	Max	Unit	Comment
	Operating Condition					
VCC	Voltage	1.9	3.0	3.6	V	
TEMP	Temperature	-20	+27	+80	ºC	
	Digital input Pin					
VIH	High level	VCC-0.3		VCC+0.3	V	
VIL	Low level	VSS		VSS+0.3	V	
	Digital output Pin					
VOH	High level (IOH=-0.25mA)	VCC- 0.3		VCC	V	
VOL	Low level(IOL=0.25mA)	VSS		VSS+0.3	V	

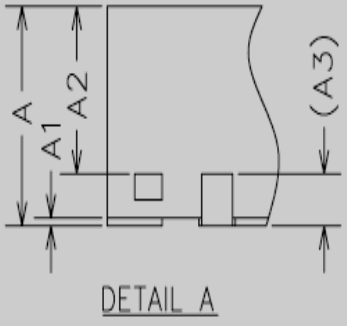
4.2 AC Performance

Name	Parameter (Condition)	Min	Typical	Max	Unit
IVDD	Deep sleep		3		uA
IVDD	Transceiver RX Full On		13		mA
IVDD	Transceiver TX Full On (0 dBm)		10		mA
IVDD	Transceiver TX Full On (5 dBm)		18		mA
IVDD	MCU at 16 MHz		8		mA
IVDD	Sleep (All Digital Retention)		9		uA
IVDD	Deep-sleep (No Retention, wake up from GPIO)		3		uA
PRF	Output power		0	5	dBm
PBW	Modulation 20 dB bandwidth		1		MHz
Max Input	1 E-3 BER	0			dBm
RXSENS	1 E-3 BER sensitivity		-89		dBm
C/I IM	Intermodulation Pin=-64 dBm		-38		dBm
C/ICO	Co-channel C/I		13		dB
C/I1ST	ACS C/I 1MHz		-1		dB
C/I2ND	ACS C/I 2MHz		-33		dB
C/I3RD	ACS C/I 3MHz		-40		dB
C/I1STI	ACS C/I Image channel		-26		dB
C/I2NDI	ACS C/I 1 MHz adjacent to image channel		-36		dB

5 Package Information







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–

6 Order Information

Part number	Package	Packing	Minimum Order Quantity
BK3431SQN32D	QFN 4mmx4mm 32-Pin	Tape Reel	3 K

7 Contact Information

Beken Corporation Technical Support Center

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Revision History

Rev.	Date	Author(s)	Remark
1.1	2015-12-23	WF	Update with BLE measurement data
1.2	2016-3-17	WF	Update with embedded FLASH
1.3	2017-4-12	MS	Added the QFN7x7 56PIN package
1.4	2017-5-4	WF	Correct the part number and MOQ
1.5	2017-9-7	WF	Keeping only QN32D package for 8Mbit FLASH